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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,124	02/11/2004	Kenichi Kawaguchi	60188-767	2618

7590 04/20/2006

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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,124	KAWAGUCHI, KENICHI	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
Supervisory PRIMARY EXAMINER
GROUP 2100
4/14/2006
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/04 and 6/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 19, 20A and 20B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1 and 9 are rejected under 35 U.S.C. 112, first paragraph, because single means claim (i.e., where a means recitation does not appear in combination with another recited element of means, therefore covering every conceivable means for achieving the stated purpose) is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph, as the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor. Please see MPEP § 2164.08 (a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Kreifels (US Patent 4,891,788).

AAPA teaches a data transfer control system connected to a bus for controlling a data transfer to a device on the bus, comprising bus cycle control (Drawings, cycle control section 105 of Fig. 19) means for performing a data write operation while maintaining a write control line of the bus in a write-enabled state (Drawings, write enabled when the byte enable register set to "0000") (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7).

AAPA does not teach the data transfer control system performing data write operation while maintaining the write control line of the bus in a write-disabled state.

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), wherein the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA's data transferring control system. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

Therefore, it would have been obvious to combine Kreifels with AAPA for the benefit of providing a truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24).

4. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Amini et al (US Patent 5,581,714).

AAPA teaches a data transfer control system and method connected to a bus for controlling a data transfer to a device on the bus, comprising:

a data storing step (Drawings, data register 143 of Fig. 19) comprising means for storing data (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7);

a transferred-word number storing step (Drawings, transferred-word number register 106 of Fig. 19) comprising means for storing the number of words of data which are to be transferred (Specification, page 1, l. 9 to page 2, l. 7); and

a bus cycle controlling step (Drawings, cycle control section 105 of Fig. 19) comprising means for controlling the data transfer such that, during a burst transfer, a write control line (byte enable register of Fig. 20A-20B) of the bus is placed in a write-enabled state (byte enable register set to "0000") and is placed in a write-disabled state

(periods when byte enable register is not set to "0000") in the other periods, and that data including a number of words which is equal to the number stored in the transferred-word number storing means is transferred while the write control line is in the write-enabled state (Specification, page 1, l. 9 to page 2, l. 7).

AAPA does not teach the data transfer control system and method connected to a bus for controlling a data transfer to a device on the bus comprising a transfer interval storing step comprising means for storing an interval between destination addresses for one-word data, wherein said transfer interval storing step stores the interval for implementing the write-enable state and the write-disable state.

Amini teaches a data transfer system and method comprising the C/BE control signal providing interval for writing between destination addresses for one-word data, wherein the writing interval implement the write-enable state (clock 3 and 6 of Fig. 2) and the write disable state (clock 1-2, 4-5 and 7 of Fig. 2) (Fig. 2 and col. 7, l. 38 to col. 9, l. 14), wherein it would be obvious to provide the storing of the writing interval in a register.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Amini's writing interval into AAPA's data transfer control system and method. The resulting combination of the references teaches the storing of the writing interval between signaling of destination addresses for one-word data.

Therefore, it would have been obvious to combine Amini with AAPA for the benefit of providing an efficient transfer of data between interconnected buses (Amini, col. 3, ll. 21-26).

5. Claim 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) and Amini et al (US Patent 5,581,714), and further in view of Sheafor et al. (US Patent 6,321,285) and Kreifels (US Patent 4,891,788).

AAPA and Amini teach all the limitation of claim 2 as discussed above, where AAPA further teaches the data transfer control system comprising:

cycle start address storing (AAPA, Drawings, cycle start address register 108 of Fig. 19) means for storing a start address of a bus cycle (AAPA, Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7); and

interrupted-cycle resuming (AAPA, Drawings, interrupted-cycle resuming section 105c of Fig. 19).

AAPA and Amini does not expressly teach the data transfer control system further comprising:

resumption address calculating means for calculating a destination address of second data when being informed by the device about interruption of the data transfer during the time when the data transfer is performed in the write-disabled state; and

means for transferring the address calculated by the resumption address calculating means to the cycle start address storing means to start a new bus cycle from the address stored in the cycle start address storing means when being informed by the device about interruption of the data transfer during the time when the data transfer is performed in the write-disabled state.

Sheafor teaches a data transfer control system comprising the interruption of the connection between the master device and the slave device, as the master device detect and thus informed by the slave device of said interruption, the master device then restart transfer of next set of data with a new address (col. 38, l. 34 to col. 40, l. 32), wherein the derivation of the new address would obvious require calculation.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Sheafor's new address upon initiation of the interrupt by the slave device into AAPA and Amini's data transfer control system. The resulting combination of the references teaches the data transfer control system further comprising upon detection of the interrupt while data transferring between the master device and the slave device, wherein the master device detect and thus informed by the slave device of said interrupt, the master device then calculate the new address and restart transfer of next set of data with the new address; and the new address would have been transferred to the cycle start address storing means as the cycle start address storing means provides the start address for the new bus cycle.

Therefore, it would have been obvious to combine Sheafor with AAPA and Amini for the benefit of proper transfer of data between master device and slave device upon detection of the interrupt in the connection initiated by either the master device or the slave device (Sheafor, col. 38, l. 34 to col. 40, l. 32).

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation

independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA's data transferring control system. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

Therefore, it would have been obvious to combine Kreifels with AAPA, Amini and Sheafor for the benefit of providing a truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24).

6. As per claim 7, AAPA, Amini, Sheafor and Kreifels teaches all the limitation of claim 3 as discussed above, where AAPA and Kreifels further teach the data transfer control system further comprising wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line (AAPA, Drawings, Data 1 transferring from data buffer to data register on Fig. 20A) when the write control line is in the write-disabled state (Kreifels, Fig. 1 and col. 1, ll. 15-24), wherein write operation is enabled while the read operation is disabled by the write-disable stated, as data are not read out to be written.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) and Amini et al (US Patent 5,581,714), and further in view of Fabre (US Patent 6,993,605).

AAPA and Amini teach all the limitation of claim 2 as discussed above, where AAPA further teaches the data transfer control system further comprising wherein the data transfer conform to the PCI standard (AAPA, Drawings, Fig. 19), it would have been obvious that data can be transfer in a plurality of modes comprising burst mode and repeat transfer of a single word data mode.

AAPA and Amini does note expressly teach the data transfer control system further comprising:

response speed storing means for storing a device response speed of a target device;

transfer speed comparing means for comparing the data transfer rate in a burst transfer mode with the data transfer rate in a data transfer mode where transfer of one-word data to a destination address is repeated, based on the values of the transfer interval storing means and the response speed storing means; and

transfer mode selecting means for selecting the burst transfer mode if the data transfer rate is faster in the burst transfer mode than in the data transfer mode where transfer of one-word data to a destination address is repeated and, if otherwise, selecting the data transfer mode where one-word data transfer bus cycle for a destination address is repeated.

Fabre teaches a data transfer control system comprising:

a table (Fig. 2, ref. 170) storing information comprising a plurality of aggregate data transfer rates and corresponding data samples, wherein said information is characterized by the time delay between data transferred and reception of response from the peripheral device (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42);

a optimizer (Fig. 2, ref. 180) comprising a comparator, base on the information stored in said table, determining the best and/or preferred aggregated data transfer rate (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42); and

selecting data sample to be use as model for future transfer (Fig. 2, ref. 185), wherein the selection would allow the specific peripheral to function at peak speed and efficiency (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Fabre's table, optimizer and selection of data sample for future transfer into AAPA and Amini's data transfer control system comprising plurality of modes of data transferring.

Therefore, it would have been obvious to combine Fabre with AAPA and Amini for the benefit of providing the peak speed and efficient rate of data transferring between the CPU (master device) and the peripheral (slave device) (Fabre, col. 7, ll. 16-58).

8. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), Amini et al (US Patent 5,581,714), Sheafor et al.

(US Patent 6,321,285) and Kreifels (US Patent 4,891,788), and further in view of Fabre (US Patent 6,993,605).

AAPA, Amini, Sheafor and Kreifels teaches all the limitation of claim 3 as discussed above, where AAPA further teaches the data transfer control system comprising wherein the data transfer conform to the PCI standard (AAPA, Drawings, Fig. 19), it would have been obvious that data can be transfer in a plurality of modes comprising burst mode and repeat transfer of a single word data.

AAPA, Amini, Sheafor and Kreifels does note expressly teach the data transfer control system further comprising:

response speed storing means for storing a device response speed of a target device;

transfer speed comparing means for comparing the data transfer rate in a burst transfer mode with the data transfer rate in a data transfer mode where transfer of one-word data to a destination address is repeated, based on the values of the transfer interval storing means and the response speed storing means; and

transfer mode selecting means for selecting the burst transfer mode if the data transfer rate is faster in the burst transfer mode than in the data transfer mode where transfer of one-word data to a destination address is repeated and, if otherwise, selecting the data transfer mode where one-word data transfer bus cycle for a destination address is repeated.

Fabre teaches a data transfer control system comprising:

a table (Fig. 2, ref. 170) storing information comprising a plurality of aggregate data transfer rates and corresponding data samples, wherein said information is characterized by the time delay between data transferred and reception of response from the peripheral device (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42);

a optimizer (Fig. 2, ref. 180) comprising a comparator, base on the information stored in said table, determining the best and/or preferred aggregated data transfer rate (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42); and

selecting data sample to be use as model for future transfer (Fig. 2, ref. 185), wherein the selection would allow the specific peripheral to function at peak speed and efficiency (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Fabre's table, optimizer and selection of data sample for future transfer into AAPA, Amini, Sheafor and Kreifels' data transfer control system comprising plurality of modes of data transferring.

Therefore, it would have been obvious to combine Fabre with AAPA, Amini, Sheafor and Kreifels for the benefit of providing the peak speed and efficient rate of data transferring between the CPU (master device) and the peripheral (slave device) (Fabre, col. 7, ll. 16-58).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) and Amini et al (US Patent 5,581,714), and further in view of Kreifels (US Patent 4,891,788).

AAPA and Amini teach all the limitation of claim 2 as discussed above, where AAPA further teaches the data transfer control system further comprising wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line (AAPA, Drawings, Data 1 transfer to Data register on Fig. 20A) when the write control line is in the write-enabled state (AAPA, Drawings, write enabled when the byte enable register set to "0000") (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7).

AAPA and Amini does not teach the data transfer control system further comprising the bus cycle controlling means drives next one-word data to be transferred onto a data line when the write control line is in the write-disabled state.

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA and Amini's data transferring control system. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

Therefore, it would have been obvious to combine Kreifels with AAPA and Amini for the benefit of providing an truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24).

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA), Amini et al (US Patent 5,581,714) and Fabre (US Patent 6,993,605), and further in view of Kreifels (US Patent 4,891,788).

AAPA, Amini and Fabre teach all the limitation of claim 4 as discussed above, where AAPA further teaches the data transfer control system further comprising wherein the bus cycle controlling means drives next one-word data to be transferred onto a data line (AAPA, Drawings, Data 1 transferring from data buffer to data register on Fig. 20A) when the write control line is in the write-enabled state (AAPA, Drawings, write enabled when the byte enable register set to "0000") (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7).

AAPA, Amini and Fabre does not teach the data transfer control system further comprising the bus cycle controlling means drives next one-word data to be transferred onto a data line when the write control line is in the write-disabled state.

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA, Amini and Fabre's data transferring control system. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

Therefore, it would have been obvious to combine Kreifels with AAPA, Amini and Fabre for the benefit of providing an truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24).

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Kreifels (US Patent 4,891,788) and Fabre (US Patent 6,993,605)

AAPA teaches a data transfer control system comprising a data write operation is performed while a write control line of a bus is in a write-enabled state; and as the data transfer control system conforms to the PCI standard (AAPA, Drawings, Fig. 19), it would have been obvious that data can be transfer in a plurality of modes comprising burst mode and repeat transfer of a single word data mode.

AAPA does not expressly teach the data transfer control system comprising bus response means for informing, when a data write operation is performed while a write control line of a bus is in a write-disabled state, reception of data earlier than in the case where the write control line is in a write-enabled state.

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA's data transferring control system. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written; and the mode of data transferring further comprises transfer of data while the control line is in the write-disable state mode and transfer of data while the control line is in the write-enable state mode.

Therefore, it would have been obvious to combine Kreifels with AAPA for the benefit of providing a truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24).

Fabre teaches a data transfer control system comprising a plurality of modes of data transferring (Fig. 2, ref 140; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42); bus response informing regarding the rate of transfer and the response time for the associated mode of data transferring (Fig. 2; Fig. 5; col. 6, l. 33 to col. 7, l. 58 and col. 9, ll. 13-42), wherein said bus response is utilized to deduce the reception of data utilizing

the first mode of data transferring is faster (earlier) or slower than the second mode of data transferring.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Fabre's determination of the faster mode of data transferring between a plurality of data transferring modes into AAPA and Kreifels' data transfer control system comprising plurality of mode of data transferring. The resulting combination of the references teaches the data transfer control system further comprising the informing which mode of data transferring is faster (reception of data earlier) among the plurality of modes of data transferring, wherein the mode data transferring comprises data transferring while the control line is in the write-disable state mode and data transferring while the control line is in the write-enable state mode.

Therefore, it would have been obvious to combine Fabre with AAPA and Kreifels for the benefit of providing the peak speed and efficient rate of data transferring between the CPU (master device) and the peripheral (slave device) (Fabre, col. 7, ll. 16-58).

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Amini et al (US Patent 5,581,714) and Kreifels (US Patent 4,891,788).

AAPA teaches a data transfer control system comprising controlling (Drawings, cycle control section 105 of Fig. 19) means for obtaining a next address where the write control line is turned into a write-enabled state (Drawings, byte enable register set to

"0000" of Fig. 20A-20B) to write a value of a signal driven onto a data line in the obtained address (Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7).

AAPA does not teach the data transfer control system, comprising

storing means for storing an interval between destination addresses of data, wherein said storing means control the shifting from the write-disable state and write-enable state; and

data write operation is performed while a write control line of a bus is in a write-disabled state.

Amini teaches a data transfer system and method comprising the C/BE control signal providing interval for writing between destination addresses for one-word data, wherein the writing interval implement the write-enable state (clock 3 and 6 on Fig. 2) and the write disable state (clock 1-2, 4-5 and 7 on Fig. 2) (Fig. 2 and col. 7, l. 38 to col. 9, l. 14), wherein it would be obvious to provide the storing of the writing interval in a register.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Amini's writing interval into AAPA's data transfer control system and method. The resulting combination of the references teaches the storing of the writing interval between signaling of destination addresses for one-word data, wherein the write interval dictates when the write-disable state will shift to the write-enable state.

Therefore, it would have been obvious to combine Amini with AAPA for the benefit of providing an efficient transfer of data between interconnected buses (Amini, col. 3, ll. 21-26).

Kreifels teaches a data transfer control system comprising a dual port FIFO, wherein said dual port FIFO can implement read operation and write operation independently (Fig. 1 and col. 1, ll. 15-24), as the dual ported FIFO can implement the write operation while the read operation is disabled.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels's dual port FIFO into AAPA and Amini's data transferring control system. The resulting combination of the references teaches the implementing the write operation into the dual port FIFO while the read operation is disabled by the write-disable stated, as data are not read from the dual port FIFO to be written.

Therefore, it would have been obvious to combine Kreifels with AAPA and Amini for the benefit of providing a truly asynchronous operation, as the write operation and be independent of the read operation (Kreifels, col. 1, ll. 15-24).

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Amini et al (US Patent 5,581,714).

AAPA teaches a data transfer control system connected to a bus for controlling a data transfer to a device on the bus, comprising:

a data storing step (Drawings, data register 143 of Fig. 19) comprising means for storing data (Drawings, Fig. 19-20B and Specification, page 1, l. 9 to page 2, l. 7);

a transferred-word number storing step (Drawings, transferred-word number register 106 of Fig. 19) comprising means for storing the number of words of data which are to be transferred (Specification, page 1, l. 9 to page 2, l. 7); and

a bus cycle controlling step (Drawings, cycle control section 105 of Fig. 19) comprising means for controlling the data transfer such that, during a burst transfer, a write control line (byte enable register of Fig. 20A-20B) of the bus is placed in a write-enabled state (byte enable register set to "0000") and is placed in a write-disabled state (periods when byte enable register is not set to "0000") in the other periods, and that data including a number of words which is equal to the number stored in the transferred-word number storing means is transferred while the write control line is in the write-enabled state (Specification, page 1, l. 9 to page 2, l. 7).

AAPA does not teach the data transfer control system connected to a bus for controlling a data transfer to a device on the bus comprising non-transfer interval storing means for storing an interval between addresses to which the data is not to be transferred, wherein said non-transfer interval storing means stores the interval for implementing the write-enable state and the write-disable state.

Amini teaches a data transfer system and method comprising the C/BE control signal providing interval for non-writing between destination addresses for one-word data, wherein the non-writing interval implement the write-enable state (clock 3 and 6 on Fig. 2) and the write disable state (clock 1-2, 4-5 and 7 on Fig. 2) (Fig. 2 and col. 7, l. 38

to col. 9, l. 14), wherein it would be obvious to provide the storing of the non-writing interval in a register.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Amini's writing interval into AAPA's data transfer control system and method. The resulting combination of the references teaches the storing of the non-writing interval between signaling of destination addresses for one-word data.

Therefore, it would have been obvious to combine Amini with AAPA for the benefit of providing an efficient transfer of data between interconnected buses (Amini, col. 3, ll. 21-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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04/05/2006

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